Area efficient System-on-Programmable-Chip Design for a Wireless Touch-Triggered Machining Probe

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Outline

- Introduction
- Probe description
- Design specifications
- SoPC components
- Verification
- Results
- Conclusions

Introduction

- Precise measurements are required in industrial applications (cutting/drilling).
- Touch probes are very popular, combined with computer numerical control (CNC) machines
  - Heidenhain/Marposs/Renishaw/Tesa
  - Wired/wireless transmission
- Size of the probe is important in order to increase the access area on the machine table
  - Wireless probes are advantageous

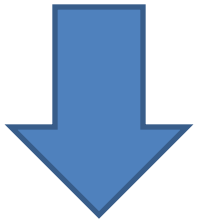
Touch-Triggered Machining Probe

- Produces a signal according to contact with the part being measured.
- PCB area inside the probe is sparse.
- Wireless probes have more complex circuitry.
- A solution that reduces PCB area would lead to an even smaller probe.

Explore a SoPC based solution to replace the existing circuitry of a touch-triggered machining probe.

System-on-Programmable Chip

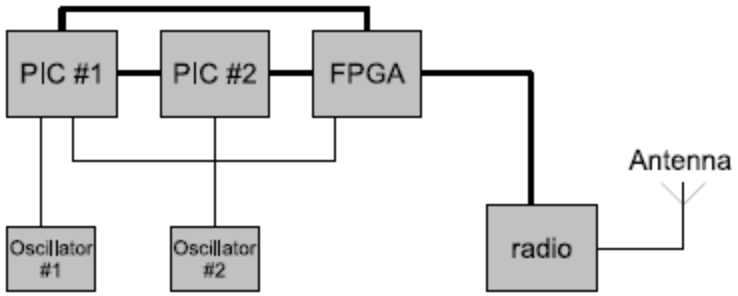
- **SoC** replaces a complete PCB with a single chip by integrating the major functionalities.
  - Once built can not be altered
- FPGAs have evolved dramatically the last decade
  - Higher densities, clock rates
  - Increased capabilities
  - Embedded processors etc



- **SoPC** is a SoC built on programmable logic (such as FPGA).
  - Structure can be modified
    - at compile time
    - or run time
  - Extremely flexible
  - Cost effective up to a certain volume

Probe Circuitry

- Main components
  - 2 x PIC microcontrollers
  - FPGA device
  - Radio transceiver



- Two crystals (second is of lower frequency) are used for normal and stand-by mode operation.
- Main PIC monitors battery/1 axis-accelerometer and controls interaction amongst components.
- Second PIC interfaces through the FPGA with strain gauges/3 axis-accelerometer.
- FPGA encodes/decodes data sent to/from wireless interface.

Design Target - Specifications

- Original PCB area occupied : 1800mm^2
  - Need to demonstrate reduction
- Software compatibility
  - code written in C for PIC18F family
- Open-source cores would be favourable.
- Overall probe power consumption.
  - No dramatic increase in power consumption
  - No figures were given

OpenCores.org

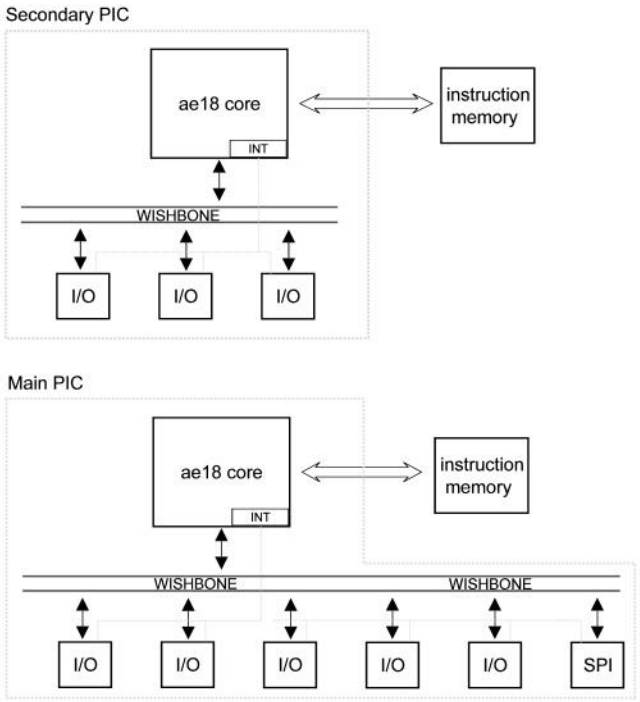
- Community for development of hardware IP cores as open source.
- Main objective is to design and publish core designs.
  - Develop standards for open source cores and platforms
  - Create tools and methods for development of open source cores and platforms
  - Develop open source cores and platforms
  - Provide documentation for these cores and platforms
- Wishbone bus (from Silicore), maintained by Opencores
  - Specification is a set of rules, recommendations /suggestions, permissions and observations.
  - Point-to-point, shared bus and crossbar switch interconnections
  - Multi-master configurations with flexible arbitration schemes
  - Standard signals + user defined signals (TAGS) to increase functionality.
  - Bridges to/from various other buses exist

SoPC components

- Processor IP
  - ae18 from *OpenCores*
    - PIC18C compatible
    - No peripherals
    - Wishbone compatible
- Processor peripherals from *OpenCores*
  - Interrupt controller (simple programmable int. controller)
  - timers/counters (PWM/Timer/Counter (PTC) module)
  - SPI interface (SPI module)
  - I/O controller (GPIO module)
- Custom functions (previously on FPGA)
  - integrated in the SoPC as dictated by the original implementation
- SoPC interconnect bus
  - Wishbone
    - Supported by *OpenCores*
    - Compatible with ae18 and all the peripherals

SoPC design - Processor Cores

- Main processor - ae18
  - 5x I/O modules
  - SPI module
  - PWM/counter/timer module
- Secondary Processor - ae18
  - 3x I/O modules
  - Interrupt controller
  - PWM/counter/timer module
- Wishbone bus used for each processor
- Module registers mapped into processors' memory

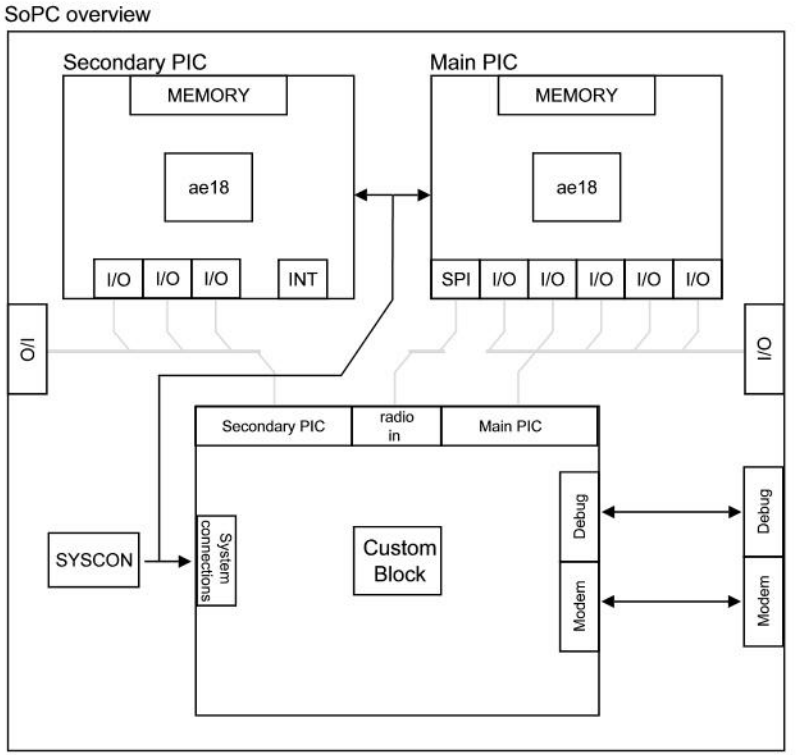


SoPC design - Interconnections

- ae18 cores connected to peripherals through wishbone bus
  - 8 bits data path
  - 12 bit address path
- Interrupt priority given to SPI module
- rest interrupts are resolved through software polling
- Memory map for module registers can be easily altered

SoPC design - Architecture

- Main/Secondary PICs written in Verilog
- Custom block written in VHDL
- PICs utilised local wishbone buses
- Custom block interfaced with PICs through I/O modules
- System Control (SYSCON) controls clock and reset signals
- Main PIC sends/receives data through the SPI interface
- Available I/O for external use
- Debug port available
- Modem interface connects to RF frontend



SoPC verification - I

- Mixed language design (VHDL&Verilog)
  - VHDL block instantiated in the higher level verilog module
    - Had to comply to some rules (supported types/generics etc.)
  - Simulators/compilers/synthesis tools are able to deal with mixed language designs
- 2 stage verification
  - Individual processors/peripherals
    - Verify bus operation
    - Access of peripherals from processors
  - Overall system verification
    - Hardware/Software co-verification

SoPC verification - II

- Stage 1
  - Test vectors to data/address bus
    - Functionality of decoders/peripherals
  - Code execution on processors
    - Check processor functionality
    - Access to peripherals
- Stage 2
  - Execute C code on both processors
    - Test interconnection with peripherals
    - Processors-custom block interaction
    - Interface with modem

SoPC implementation

- FPGA realisation instead of ASIC
  - Ease of implementation
  - Cost effective (depends on production volume)
  - Flexibility of design
- Devices considered
  - Xilinx
    - Virtex 4/5, Spartan 3
  - Altera
    - Cyclone I/II/III
  - Actel
    - Fusion

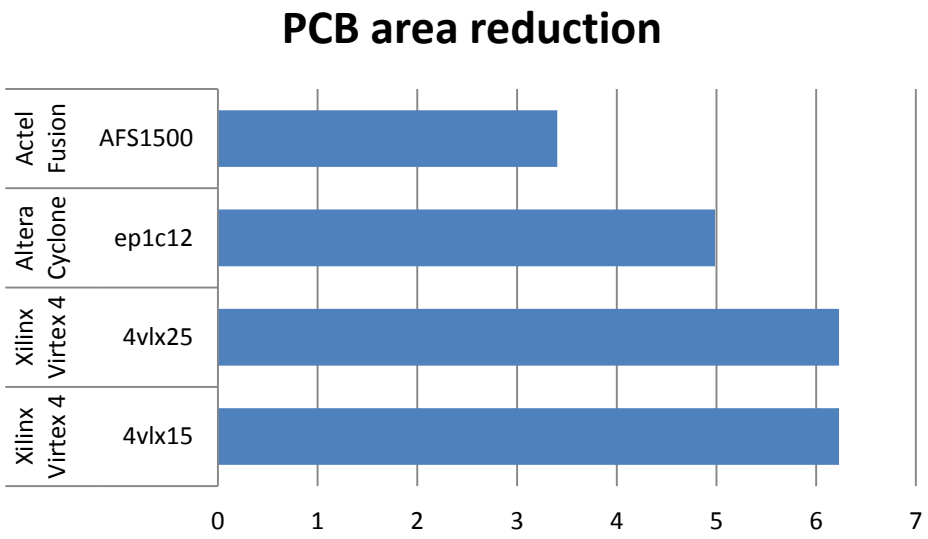
Results - I

- FPGAs that accommodated the SoPC

Family	Model	Package (I/O pins)	Area (mm^2)
Xilinx Virtex 4	4v1x15	sf363(240)	289
Xilinx Virtex 4	4v1x25	sf363(240)	289
Altera Cyclone	Ep1c12	f324(249)	361
Actel Fusion	AFS1500	fg484(223-40)	529

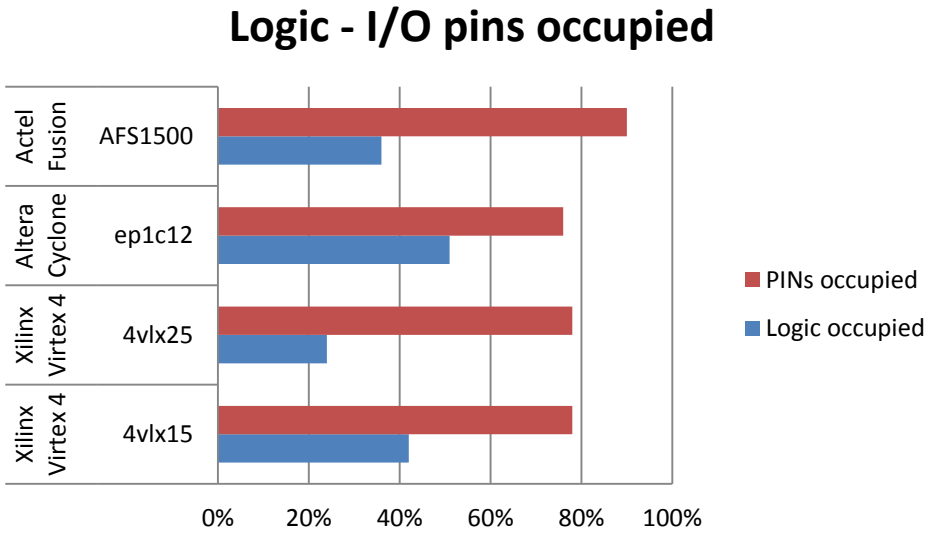
- **PCB area reduction achieved**
- **Less layers for routing needed**
- **Flexibility – future updates in hardware**
- **Compatibility with original software**

Results - II



- FPGAs that could fit the SoPC and provide area benefit
- More than 6x reduction
- Actel Fusion has also embedded some analogue functionality (for future use)

- Plenty of logic for future use available
- High I/O pin use
  - could multiplex signals and save on pins



Conclusions – Future work

- Achieved 6x area reduction
- Simplicity in PCB assembly (1 IC vs 3 ICs)
- Using FPGAs for size reduction is not intuitive
  - Can be proven beneficial in some cases
  - Additional degree of freedom for future design updates

ALTERNATIVES

- ASIC to incorporate RF functionality and further reduce size
- Single multi-threaded processor to substitute the PICs
- Use of FPGA embedded processor
  - Would require re-write of software

Thank you.
Any questions?

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